Remarks/Arguments:

Paragraph [0064] of the specification is amended to correct a reference number. The implant is erroneously identified in the specification as filed as "466." This reference is changed to "494" to be consistent with the drawing Fig. 4D which provides the basis for this amendment.

Claims 1, 3, 7-11, 13-18, 20, 21, 31 and 32 are pending in the above-identified application. Claims 1, 11 and 18 are amended to emphasize features that are already present in the claims. In particular, claim 1 is amended to emphasize that the charge wells are formed in the substrate of the first conductivity type, that these charge wells are separated by an inter-electrode gape in the substrate of the first conductivity type and that the semiconductor region of the first conductivity type is formed in the inter-electrode gap. These limitations were already in claim 1 which stated that the substrate is of a first conductivity type, that the two charge wells are formed in the substrate and separated by an inter-electrode gap and that the semiconductor region is of the first conductivity type and in the inter-electrode gap. The amendments were made because it appears that the Examiner did not understand these limitations. In the Office Action the Examiner asserted that these limitations were not found in the claims. As these limitations concern elements already in the claims, they do not affect the claim scope.

Claims 1 and 32 were rejected under 35 U.S.C. § 102(b) as being anticipated by Fujii. This ground for rejection is respectfully traversed. In particular, Fujii does not disclose or suggest:

> a dielectric layer overlaying at least a portion of the substrate, the dielectric layer being a CMOS gate dielectric layer
>
> at least two gate electrodes overlaying the dielectric layer, the at least two gate electrodes configured to define at least two charge wells in the substrate of the first conductivity type, in response to a bias potential applied to the at least two gate electrodes, the at least two gate electrodes being separated by an inter-electrode gap in the substrate of the first conductivity type; and
>
> apparatus for stabilizing the inter-electrode gap selected from a group consisting of:
>
> a semiconductor region of the first conductivity type, formed in the inter-electrode gap, but having a different dopant concentration than the substrate; and

means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes.

In item 3 of the Office Action, the Examiner asserts that Fujii teaches "the at least two gate electrodes (42, 44) overlaying the dielectric layer, the at least two gate electrodes configured to define at least two charge wells (the n and p regions of the substrate), the at least two gate electrodes being separated by an inter-electrode gap (the gap between 42 and 44) and apparatus for stabilizing the inter-electrode gap, is a semiconductor region (36) of the first conductive type but having a different dopant concentration than region (32), in the inter-electrode gap."

Applicants respectfully disagree with this assertion, because Fujii clearly shows in FIGs. 8 and 9 that the second p-type silicon region 36 (i.e., which the Examiner corresponds to the semiconductor region of the first conductive type recited in claim 1) is of opposite type to the n-type material in which the charge wells are formed. The subject invention, as defined by claim 1, requires that the charge wells formed by the gate electrodes be formed in the substrate of the first conductivity type and that the stabilizing implant also be of the first conductivity type. Fujii does not meet this limitation because, in Fujii, the charge wells are formed in the n-type layer 32 while the implants 36 are p-type implants. This claim limitation is illustrated in Fig. 4D of the subject application in which the charge wells are formed in the n-type region 110" and the stabilizing implant is an n-- implant 494. (See paragraph [0064] of the subject application).

In addition, Fujii fails to disclose that the dielectric layer overlying at least a portion of the substrate is a CMOS gate dielectric layer. Indeed, Fujii relates to a CCD process. As set forth in the subject specification at paragraph [0007], CCD and CMOS processes have been incompatible. An advantage of the subject invention is that it allows CCD devices to be built using standard CMOS processes and, as defined by claim 1, a CMOS gate dielectric layer is the dielectric layer of the charge-coupled device. Accordingly, the use of a CMOS gate electrode provides the subject invention with an advantage over Fujii. Because, as set forth in the subject specification, CMOS and CCD devices are incompatible, it would not have been obvious to the skilled person to make the dielectric layer in Fujii as a CMOS gate dielectric layer.

As claim 1 requires the substrate to be formed of the first conductivity type, the charge wells to be formed in the substrate, the implant layer to be also of the first conductivity type, and the dielectric layer to be a CMOS gate dielectric layer, claim 1 recites structure that is not found in Fujii. Accordingly, claim 1 is not subject to rejection as being anticipated by Fujii.

Dependent claim 32 includes all of the features of claim 1 from which it depends. Thus, claim 32 is not subject to rejection under 35 U.S.C. § 102(b) as being anticipated by Fujii for the reasons set forth above concerning the rejection of claim 1.

Claims 20 and 21 were rejected under 35 U.S.C. § 102(e) as being anticipated by Savoye. This ground for rejection is respectfully traversed. In particular, Savoye does not disclose or suggest:

> a well region of a second conductivity type, opposite to the first conductivity type, formed in the front side of the substrate and separate from the photodetector, the well region and the substrate forming a semiconductor junction; and
>
> at least one diffusion region in the well region of the second conductivity type forming a component of the back illuminated imager;
>
> whereby the component of the back illuminated imager is shielded from photocarriers generated in response to photons received at the back side of the substrate by the semiconductor junction.

In the Office Action, it is asserted that Savoye teaches "a well region (420) of a second conductivity type, opposite to the first conductivity type (n region), formed in the front side of the substrate and separate from the photodetector, the well region and the substrate forming a semiconductor junction (refer to fig. 4B); and at least one diffusion region (400) in the well region of the second conductivity type forming a component of the back illuminated imager; whereby the component of the back illuminated imager is shielded from the photocarriers generated in response to photons received at the back side of the substrate by the semiconductor junction (refer to col. 16, lines 6-17)." Contrary to the assertion by the examiner, Savoye teaches that the component of the back illuminated imager is formed in a buried channel 70, not in the heavily-doped p-type region 420. Thus, Savoye requires an extra step that is not used in the subject invention. Referring to Fig. 4D, the subject invention forms a p-well 493 in the n- substrate 110" and it is the junction between the p-well and the n-substrate that shields the diffusion regions 495, 496 and 497 from the photocarriers. Savoye,

on the other hand, forms the buried channel 70, and forms the blooming drain 400 in the channel 70. Savoye needs an additional implant 420 to block the photocarriers from the blooming drain. This additional implant can not be the well region of the subject invention because the component of the back illuminated imager is not formed in this region.

Savoye teaches that the p-n junction between the buried channel 70 and the substrate is insufficient to shield the blooming drain from the photoelectrons. (See col. 16, lines 14-17). Thus, Savoye teaches away from the invention defined by claim 20. Because the subject invention achieves the same effect without requiring the additional heavily-doped p-type region 420 required by Savoye, the subject invention represents an advantage over Savoye. Moreover, because Savoye teaches that the junction between the buried channel 70 and the substrate is insufficient to shield the blooming drain 400, the skilled person would not be motivated to modify Savoye to meet the limitations of claim 20.

Because Savoye does not disclose or suggest a well region that both includes a component of the back illuminated imager and that forms a p-n junction with the substrate that shields the component from photocarriers, as required by claim 20, claim 20 is not subject to rejection under 35 U.S.C. § 102(e) in view of Savoye. Claim 21 depends from claim 20 and is not subject to rejection under 35 U.S.C. § 102(e) in view of Savoye for at least the same reasons as claim 20.

Claims 3, 7, 8-11, 13-15, 18 and 31 were rejected under 35 U.S.C. § 103(a) as being obvious in view of Fujii and Ohsawa et al. This ground for rejection is respectfully traversed. In particular, neither Fujii, Ohsawa et al. nor their combination discloses or suggests:

> a dielectric layer overlaying at least a portion of the substrate, the dielectric layer being a CMOS gate dielectric layer
>
> at least two gate electrodes overlaying the dielectric layer, the at least two gate electrodes configured to define at least two charge wells in the substrate of the first conductivity type, in response to a bias potential applied to the at least two gate electrodes, the at least two gate electrodes being separated by an inter-electrode gap in the substrate of the first conductivity type; and
>
> apparatus for stabilizing the inter-electrode gap selected from a group consisting of:

a semiconductor region of the first conductivity type, formed in the inter-electrode gap, but having a different dopant concentration than the substrate; and

means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes

as required by claim 1,

a dielectric layer overlaying at least a portion of the substrate, the dielectric layer being a CMOS gate dielectric layer;

at least two gate electrodes overlaying the dielectric layer, the at least two gate electrodes defining at least two charge wells, in the substrate, in response to a bias potential applied to the at least two gate electrodes , the at least two gate electrodes being separated by an inter-electrode gap; and

means for stabilizing the inter-electrode gap including means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes to stabilize the inter-electrode gap by preventing charge barriers from interfering with charge transfer between adjacent gate electrodes,

as required by claim 7,

a first dielectric layer overlaying the semiconductor layer, the first dielectric layer being a CMOS gate dielectric layer;

at least two gate electrodes overlaying the first dielectric layer and configured to define at least two charge wells, respectively, in the semiconductor layer, in response to a bias potential applied to the at least two gate electrodes, wherein adjacent ones of the at least two gate electrodes are separated by an inter-electrode gap in the semiconductor layer, a combination of one of the at least two charge wells and its respective overlaying gate electrode forming a photogate optical sensor and a combination of another one of the at least two charge wells and its respective overlaying gate electrode forming a transfer gate; and

apparatus for stabilizing the inter-electrode gap selected from a group consisting of:

a semiconductor region of the first conductivity type, formed in the inter-electrode gap, but having a different dopant concentration than the semiconductor layer; and

means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend

across the inter-electrode gap from at least one of the at least two gate electrodes

as required by claim 11, or

an oxide layer formed over at least the well region, the oxide layer being a CMOS gate oxide layer;

first and second polysilicon gate electrodes formed on the oxide layer over the well region, the first and second gate electrodes being separated by an inter-electrode gap in the well region, wherein the combination of the first and second polysilicon gate electrodes, the oxide layer and the well region form a buried channel CCD register; and

apparatus for stabilizing the inter-electrode gap selected from a group consisting of:

a semiconductor region of the second conductivity type, formed in the inter-electrode gap of the well region, but having a different dopant concentration than the well region; and

means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes

as required by claim 18

Fujii is described above. Ohsawa et al. was cited as showing the further gate electrode overlying the further dielectric layer as required by claim 3, which depends from claim 1. The combination of Fujii and Ohsawa et al was cited as inherently disclosing the "means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes," as required by claims 1, 7, 11 and 18. Applicants respectfully disagree that the combination of Fujii and Ohsawa et al. inherently disclose this feature of claims 1, 7, 11 and 18. In particular, Applicants note that Ohsawa et al. disclose the further gate electrode overlying the further dielectric layer to control the inter-electrode gap. By disclosing this feature, Ohsawa et al. admit that their gate electrodes and driving circuitry do not form the fringing fields because, if it did, then the further gate electrode overlying the further dielectric layer would not be needed. Fujii discloses virtual gate regions 34 and 36, shown in Fig. 9, which have the effect of eliminating the need for stabilizing any inter-electrode

gap, as described in the specification of the subject invention at paragraphs [0050] and [0051], with reference to Fig. 3B. As stated in these paragraphs, this is a known structure.

Because both Fujii and Ohsawa et al. disclose either structures that do not need to have inter-electrode gaps stabilized or structures, other than the claimed structure, that stabilize the inter-electrode gap, the combination of these references can not "inherently" disclose the structures required by claims 1, 11 and 18.

The requirements for an item to be inherent in a disclosure are well settled. The CCPA had stated that "inherency ... may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Oelrich*, 666 F.2d. 578, 581, 212 USPQ 323, 326 (CCPA 1981). That is, the missing element or function must necessarily result from the prior art reference(s). In this instance, because these references either do not need to stabilize the inter-electrode gap or disclose other methods than the claimed method to stabilize the gap, the skilled person would not recognize that the "means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes," as being present in either reference or their combination.

Furthermore, Applicants continue to assert that the combination of Fujii and Ohsawa et al. is improper. "[T]he mere fact that a worker in the art could rearrange the part of the reference device to meet the terms of the claims on appeal is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary change in the reference device." See *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984).

A prima facie obviousness rejection requires that the modification of one reference be based on motivation evidenced in the record. Because the cited references either do not need to stabilize the inter-electrode gap or use other methods for stabilizing the gap, the cited art does not provide any suggestion or motivation to modify Fujii to control gap potential to cause a fringing field to extend across the inter-electrode gap to suitable stabilize the inter-electrode gap. Thus, a rejection based on the rationale given by the Examiner is improper.

Accordingly, claims 1, 7, 11 and 18 are not subject to rejection as being unpatentable over Fujii in view of Ohsawa et al. Claims 3 and 8-10 depend from claim 1 and claims 13-15 and 31 depend from claim 11. Accordingly, these claims are not subject to rejection as being unpatentable over Fujii in view of Ohsawa et al. for at least the same reasons as their base claims.

Claims 16 and 17 were rejected under 35 U.S.C. § 103(a) as being obvious in view of Hieda and Fujii. This ground for rejection is respectfully traversed. In particular, neither Hieda, Fujii nor their combination disclose or suggest,

> a single monolithic integrated circuit including:
>
> a charge coupled device (CCD) imager array; and
>
> a complementary metal oxide semiconductor (CMOS) analog to digital converter coupled to receive image signals from the CCD imager array

as required by claims 16 and 17. In the Office Action, it was asserted that Hieda discloses "a single monolithic integrated circuit including CCD imager (2) (fig.1) and a CMOS analog to digital converter (3)." Applicants respectfully disagree with this assertion. Hieda, at col. 3, lines 23-29 states:

> Referring to FIG. 1, this image pickup apparatus comprises an image pickup optical system 1 including an image pickup lens and a stop, a CCD 2 which is a color image sensor, and a digitization circuit 3 which converts a CCD output signal into a digital signal by using a sample-and-hold circuit, a gain variable amplifier, and an A/D converter. These components of the digitization circuit 3 are formed on a one-chip IC.

This statement by Hieda concerning the circuitry formed on the "one-chip IC" refers only to the components of the digitization circuit 3, not to the CCD 2. Thus, contrary to the statement in the Office Action, Hieda does not teach that a CCD imager and a CMOS analog-to-digital converter can be formed on a single monolithic integrated circuit. Furthermore, as set forth in the specification at paragraph [0007] it is not feasible to fabricate known CCD devices using CMOS process techniques. Also, it is noted that the Fujii reference does not even mention CMOS, Complementary Metal Oxide Semiconductor or any similar circuitry. From the above, based on Hieda and Fujii, the skilled person would not understand that a CMOS analog-to-digital converter could be combined with a CCD imager on a single monolithic integrated circuit,

as required by claims 16 and 17. Accordingly, claims 16 and 17 are not subject to rejection under 35 U.S.C. § 103(a) as being obvious in view of Hieda and Fujii.

In view of the foregoing amendments and remarks, Applicants request that the examiner reconsider and withdraw the rejection of claims 1, 3, 7-11, 13-18, 20, 21, 31 and 32.

Respectfully submitted,

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